Measurement-Based Model Parameters for Quasi-Optical Electron Device Arrays

L. B. Sjogren, H.-X. L. Liu, X.-H. Qin,
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Abstract—**Impedance element values for a Schottky beam control diode array are obtained by curve-fitting quasioptical reflection coefficient measurements to a series *RLC* array model. The model provides a good representation of the array behavior. Parameters of Schottky varactor arrays tested to-date are summarized. The technique should be applicable to other quasioptical arrays, as well.**

I. Introduction

Planar arrays of integrated semiconductor devices have attracted recent interest as solid state components for high frequency quasioptical applications. In order to fully realize the potential of quasioptical device arrays, accurate models must be developed. Successful models for high frequency electron devices have been obtained by "de-embedding" the elements of a physical model from measured device behavior (e.g. measured S parameters). This procedure is equally applicable to quasioptical arrays. In [1], the model parameters of a Schottky varactor diode array were successfully extracted from complex transmission coefficient measurements. In the current paper, we perform a similar parametric extraction on a new array by the use of complex reflection coefficient measurements, and summarize the performance of Schottky varactor diode arrays tested to-date.

II. Characterization

The behavior of a diode array (whose unit cell is illustrated in Fig. 1) can be represented by a shunt impedance across a transmission-line representing a (normally-incident) propagating beam whose electric field is parallel to the diode embedding strip. For the varactor array, the impedance consists of an inductor (due to the strip) in series with a capacitor and resistor (the latter two primarily associated with the diode). In [1], the values of R, L, and C in this series-resonant model were obtained for a varactor array denoted "PS1" by extraction from quasioptical transmission coefficient measurements.

A new array, denoted "PS2", with 7000 operational "ABD" [2] Schottky diode varactors, has been characterized here by use of reflection coefficient measurements. (Dimensions of the PS2 array are $a = 300$ μm, $b = 120$ μm, and $w = 10$ μm. Further details on the design and functional operation of the array can be found in [3], [4].) The phase of the reflection coefficient was obtained by the method of [5]. In this technique, a portion of the incident beam is aligned perpendicular to the diode embedding strips, serving as a reference beam. The reflection phase for the "active" beam (polarized parallel to the diode strips) can then be determined by examining the polarization state of the reflected beam. The amplitude is obtained by comparison of the reflected beam power versus that at a frequency for which there is no attenuation, with a beam component polarized perpendicularly to the "active" array axis employed as an amplitude reference to account for variation of incident beam power versus frequency. The array configuration for the reflection tests is shown in Fig. 2.

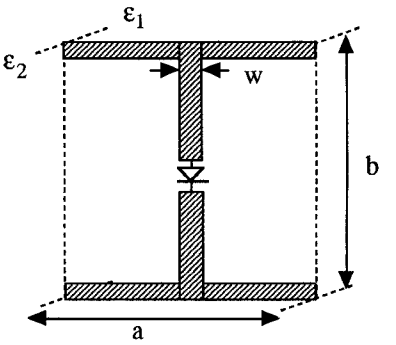

Fig. 1. Schematic illustration of a beam control array unit cell. A normally incident beam, with vertically polarized electric field, induces a current through the vertical strip and diode. The horizontal (bias) lines have essentially no effect on array behavior.

A. Array Resistance

At frequencies for which the thickness of the reflector-backed substrate equals an odd multiple of a quarter wavelength, the array impedance appears directly as a load termination. At this frequency, reflection amplitude is a much stronger function of array resistance than array reactance. The measured power reflectance of the PS2 array is shown on Fig. 3. Comparison with curves obtained by transmission-line circuit simulation (using approximate estimates for L and C) shows that a "fit" is obtained for a PS2 array resistance of approximately 75 Ω. The same test, applied to a PS1 array, shows an approximate resistance of 35 Ω. This agrees closely with the transmission test result [1] of 40 Ω. The high resistance of the PS2 array was due to extreme thinning of the Schottky anode metallization, which was verified by microprobe measurement of the DC resistance of the Schottky anodes on typical diodes. These measurements indicated an anode finger resistance of 12 Ω. With two anode fingers per ABD, and the array resistance due to the array device being that of the individual device times the aspect ratio of the unit cell, a/b [6], the anode finger will contribute 60 Ω to the array resistance, dominating the array resistance. The resistance of a well-fabricated ABD should be very low; design and process modifications are proposed in [2] which should assist in achieving a low resistance ABD.

B. Array Inductance

Parameter extraction for the PS1 array showed [1] that the inductance obtained by electromagnetic simulation is very accurate. Thus, for the PS2 array, the simulated value of 160 pH has been assumed.

C. Array Capacitance

Measurements of reflectance and reflection coefficient phase were taken at three frequencies centered at the "flat amplitude frequency". The array capacitance was determined as the value which, employed in a quasioptical transmssion line circuit simulation, provides a least-squares fit with the measured results. The fitting was performed independently for the set of reflectance and reflection phase curves.

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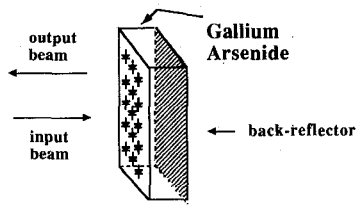

Fig. 2. Array configuration for reflection testing. Addition of a "shim" layer of GaAs gives a nominal array thickness of 0.838 mm. Behavior of the array indicated actual thickness of 0.851 mm, and this value was assumed for model parameter fitting.

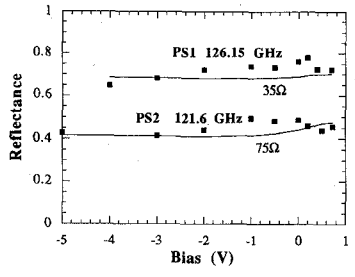

Fig. 3. Beam reflectance for the PS1 and PS2 arrays at the "flat amplitude" frequency (PS1: 126.15 GHz, PS2: 121.6 GHz). Markers indicate measured values; lines indicate the simulated results with "best fit" model parameters.

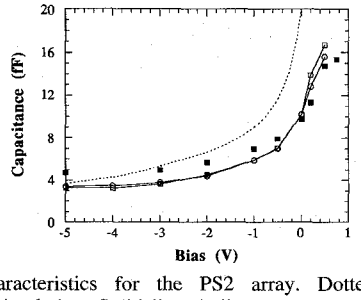

Fig. 4. C-V characteristics for the PS2 array. Dotted line: original one-dimensional simulation. Solid line (hollow squares): 1-MHz C-V curve for typical array diode. Solid line (hollow circles): 1-MHz C-V curve for typical array diode. Solid line (hollow circles): 1-MHz C-V characteristic of an "array bias unit" [4] (group of contiguous rows of diodes), with coplanar strip capacitance subtracted [1], scaled to a single diode. All three curves are divided by the aspect ratio a/b for direct comparison with the quasioptical C-V results, which are shown by solid markers.

The two resultant extracted C-V curves agreed well. The "true" C-V curve was taken as the average of the two. In Fig. 4, the extracted C-V curve is shown, along with that of the original simulation (one dimentional solution for Poisson's equation) and the results for a typical diode measured at 1 MHz with a C-V meter (measured as described in [1]).

III. Conclusion

Figs. 5 and 6 show that the *RLC* array model, with "best fit" parameters, provides a good representation of the array behavior. The greatest deviation is for the phase at negative bias, where a small change (or error) in capacitance results in a large phase difference. These results show that reflection coefficient measurements can be successfully employed in the parametric characterization of quasioptical active arrays. Desirable future extensions include the use of measurements at a larger number of frequencies, including more elements for a more precise model, and the extension of the procedure for more complex arrays, such as amplifier arrays [7].

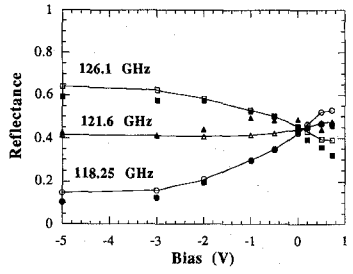

Fig. 5. Beam (power) reflectance curves for the PS2 array. Solid markers indicate measured values; lines indicate the simulated results with "best fit" model parameters.

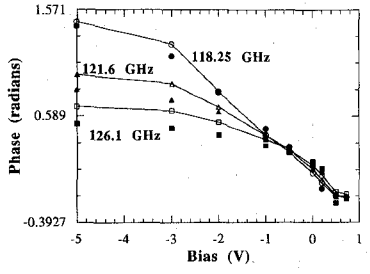

Fig. 6. Reflected beam phase curves for the PS2 array. Solid markers/dashed lines indicate measured values; hollow markers/solid lines indicate the simulated results with "best fit" model parameters. Phase is with respect to a reference to a reference plane at the air to GaAs interface, and is relative to that of an orthogonally polarized beam (3.08 radians).

TABLE I
Model Parameters of the Beam Control Arrays. *Two Arrays were Tested; However, C-V Curves are Available Only for the Array with the Higher Resistance

Design	C_{min} (fF)	c_{rd}	η_{qo}	R_{array} (Ω)
[8]	17.5	3.29	0.630	78, 26*
PS1	4.9	6.35	0.395	35
PS2	4.7	5.12	0.613	75

Performance-related parameters for Schottky varactor arrays fabricated to-date are summarized in Table I. Estimated values from the original proof-of-principle experiment [8] are included. A useful performance parameter is the ratio of array capacitance ratio, $c_{r,a}$, ($c_r = C_{max}/C_{min}$) to diode capacitance ratio, $c_{r,d}$, which we denote the quasioptical efficiency, η_{qo}. (Note that $c_{r,a}$ is based on the slightly larger maximum useable bias obtainable at the millimeter-wave frequency versus that for the 1 MHz C-V test, due to the smaller relative conductance versus capacitive susceptance at the higher frequency). The quasioptical efficiency can be considered a gauge of how effectively the performance range of the diode is achieved by the array as a whole. Its value is considerably better for the PS2 array than the PS1 array, which is consistent with the achievement of greater capacitance uniformity over the array and lower incidence of faulty cells [3]. Both arrays achieve a very low minimum capacitance (approximately 5 fF), which can be attributed to the rectangular unit cell design [6].

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MIM Capacitor Modeling: A Planar Approach

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***Abstract*—On the basis of a planar approach, an equivalent circuit model of MMIC overlay capacitors with feeding lines in generic position has been derived. Closed expressions for the equivalent circuit elements are presented. The validity of the proposed circuit has been successfully tested with experimental data. Its simplicity and flexibility makes it attractive for implementation in CAD packages.**

I. Introduction

Metal–Insulator–Metal (MIM) capacitors are key elements in many microwave and millimeter-wave monolithic integrated circuits. DC-blocks, matching sections, and biasing circuitry widely utilize this component. An accurate model of the structure is therefore crucial for any MMIC design. Many monolithic foundries have developed their own proprietary models by means of parameter extraction methods from experimental data. The so-obtained models are too device-specific and their validity is restricted to the frequency range of the fitting measurements. Other approaches, closer to the physical structure of the MIM capacitor, have been previously presented, resulting in a distributed [1] or lumped [2] equivalent model. Both approaches are zero- or mono-dimensional and therefore do not take into account the intrinsic planar behavior of the structure, demonstrated in [3] and [4]. Such a planar behavior must be accounted for when, due to layout constraints, the designer is forced to feed the capacitor with off-centered ports or even positioned on perpendicular sides of the structure.

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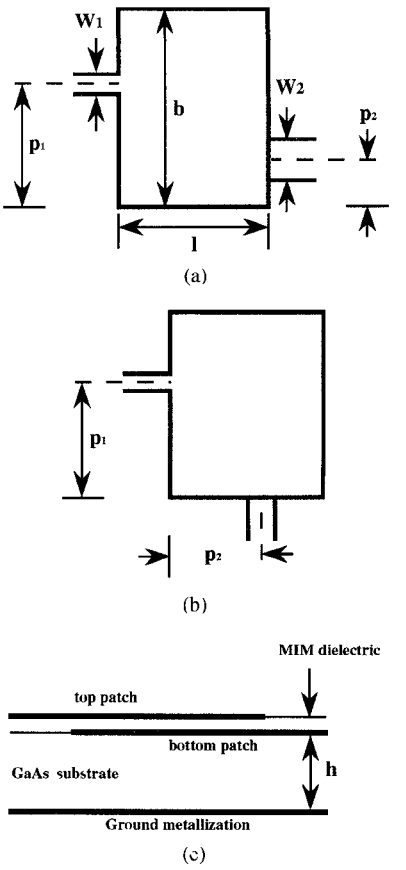

Fig. 1. The MIM capacitor: (a) top view for feeding lines on opposite sides; (b) perpendicular sides; and (c) section of the structure.

Moreover, design considerations suggest the development of a circuit model of the MIM capacitor that can be easily implemented in commercial CAD packages. To fulfill these requirements, in this paper a novel circuit model, based on a planar approach, for two-port overlay capacitors is presented. The model accounts for the effects of generic port positioning: the ports can be placed on opposite sides of the structure and off-centered or even on perpendicular sides. Simple and closed-form expressions for the model elements are provided. The proposed model has been successfully tested comparing the simulated results to experimental data in a wide frequency band.

II. The Equivalent Circuit

The typical structure of an MIM capacitor is shown in Fig. 1. The prevailing effect at very low frequencies is by far the capacitive one: it can be easily represented by a series-connected parallel-plate capacitor. As frequency increases, planar effects due to the bottom patch, which are not taken into account by this simple model, become evident, altering the ideal capacitive behavior. This leads us to model the whole structure as a cascade connection of the main series capacitor (C_{MIM}, whose value can be computed as if it were a parallel-plate capacitor) and of the bottom patch, added to account for the above-mentioned planar effects.

As already well established (see [5]), the external behavior of such a planar structure can be modeled in terms of a Z-matrix description. The entries Z_{ijR} are obtained enclosing the patch by lateral magnetic walls and expanding the EM field inside the resulting resonator into